Vignesh Balaji

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Research Interests

Architectural/Software Optimizations for Irregular (Graph Processing) Workloads, Cache Coherence Protocols, Approximate Computing

Education

2015 - **Carnegie Mellon University, Pittsburgh**
PhD in Electrical and Computer Engineering
Advisor: Brandon Lucia
Field: Computer Architecture
Expected Graduation: **May 2021**

2011-2015 **Birla Institute of Technology and Science (BITS) Pilani, India**
B.E. (Hons.) in Electronics and Instrumentation
Thesis: *Design of a resource tracker for a runtime reconfigurable coprocessor*
GPA: 9.34/10 (Department Rank: 1)

Research Experience

Sep 2015 - Present **Carnegie Mellon University**
Graduate Research Assistant
My research focuses on architectural and software optimizations for sparse, irregular memory access workloads (particularly, graph analytics). A fundamental tenet of the research has been to leverage the unique properties of graph analytics workloads and input graphs to design locality and scalability optimizations for efficient graph processing on multi-core processors.

Jan 2015 - May 2015 **Indian Institute of Science (IISc), Bangalore**
Project Assistant
For my undergraduate thesis, I designed the simulation infrastructure to model a resource availability tracker used for scheduling kernels on a dynamically reconfigurable polymorphic coprocessors (REDEFINE).

Professional Experience

May 2019 - Aug 2019 **Intel Labs, Santa Clara**
Summer Intern
Explored optimizations for streaming sparse tensor factorization by leveraging temporal characteristics of real-world input tensors.

May 2018 - Aug 2018 **Nvidia Architecture Research Group (ARG), Massachusetts**
Summer Intern
Developed analytical models for an accelerator targeting graph processing and sparse linear algebra. The analytical models were used to explore the trade-off space for on-chip buffer management on the accelerator.

May 2014 - Aug 2014 **IBM Semiconductor Research and Development Centre (SRDC), Bangalore**
Summer Intern
Explored different organizations for Tunnel Field Effect Transistors (TFETS) to produce similar output responses as a CMOS transistors.

May 2013 - Aug 2013 **IGCAR, Kalpakkam**
Summer Intern
Designed a SoC-based system to detect the health of an electrochemical hydrogen sensor deployed in a Fast Breeder Test Reactor.

Publications

- **P-OPT: Practical Optimal Cache Replacement for Graph Analytics**
  Vignesh Balaji, Neal Crago, Aamer Jaleel, Brandon Lucia
  Paper in International Symposium on High Performance Computer Architecture (HPCA) 2021
  (Nominated for Best Paper Award)

- **Optimizing Graph Processing and Preprocessing with Hardware Assisted Propagation Blocking**
  Vignesh Balaji, Brandon Lucia
  ArXiv 2020

- **Peacenik: Architecture Support for Not Failing Under Fail-Stop Memory Consistency**
  Rui Zhang, Swarnendu Biswas, *Vignesh Balaji*, Michael D. Bond, and Brandon Lucia
  Paper in International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020

- **Combining Data Duplication and Graph Reordering to Accelerate Parallel Graph Processing**
  Vignesh Balaji, Brandon Lucia
  Paper in International Symposium on High-Performance Parallel and Distributed Computing (HPDC) 2019

- **When is Graph Reordering an Optimization?**
  Vignesh Balaji, Brandon Lucia
  Paper in IEEE International Symposium on Workload Characterization (IISWC) 2018
  (Won the Best Paper Award)

- **Flexible Support for Fast Parallel Commutative Updates**
  Vignesh Balaji, Dhruva Tirumala, Brandon Lucia
  (ArXiv 2017)

- **An Architecture and Programming Model for Accelerating Parallel Commutative Computations via Privatization**
  Vignesh Balaji, Dhruva Tirumala, Brandon Lucia
  Poster presented as part of PPoPP 2017

- **Intermittent Computing: Challenges and Opportunities**
  Brandon Lucia, *Vignesh Balaji*, Alexei Colin, Kiwan Maeng, Emily Ruppel
  Paper in Summit on Advances in Programming Languages (SNAPL) 2017

- **Overcoming the Data-flow Limit on Parallelism with Structural Approximation**
  Vignesh Balaji, Brandon Lucia, Radu Marculescu
  Paper presented in Workshop on Approximate Computing (WAX) 2016, co-located with ASPLOS 2016

Relevant Coursework

- **Computer Architecture** (18-740, Fall 2015)
- **Energy Aware Computing** (18-743, Fall 2015)
- **Machine Learning** (10-701, Spring 2016)
- **Optimizing Compilers for Modern Architectures** (10-701, Spring 2016)
- **Advanced and Distributed Operating Systems** (15-712, Fall 2016)
- **Networks in the Real World** (18-755, Fall 2016)
- **Parallel Computer Architecture** (18-742, Spring 2017)

Honors

- **Best Paper Nominee, HPCA** 2021
- **Best Paper Award, IISWC** 2018
- **Deans Fellowship, Carnegie Mellon University** 2015
- **Merit Scholarship, BITS Pilani** 2013 & 2014

Service

- **Shadow Program Committee:** ASPLOS 2018
- **Reviewer, IEEE Transaction on Computers:** Special Issue on Domain-Specific Architectures for Emerging Applications 2019

Skills

- **Languages:** C++, C, Python, x86 assembly, MATLAB
- **Tools/Simulators:** Pin, Sniper, Gem5, perf, Intel VTune, Intel PCM, PAPI, LIKWID